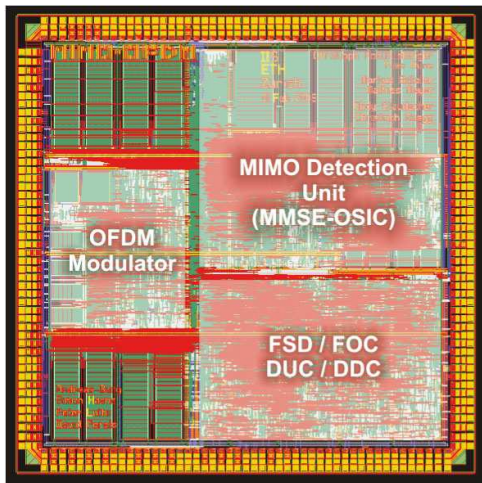


# IIS ASICs for Wireless MIMO Communication - Part 1

## 4-Stream MIMO Transceiver



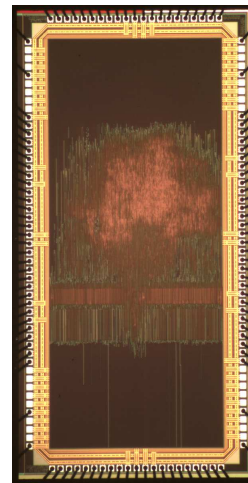
### Description

- First 4-stream MIMO transceiver ASIC

### Technical Data

- Process: UMC 0.25  $\mu\text{m}$  1P/5M CMOS technology
- Clock: 80 MHz
- Area: 12.8 mm<sup>2</sup>
- Achieves 192 Mbit/s in 20 MHz bandwidth

## Programmable LDPC Decoder



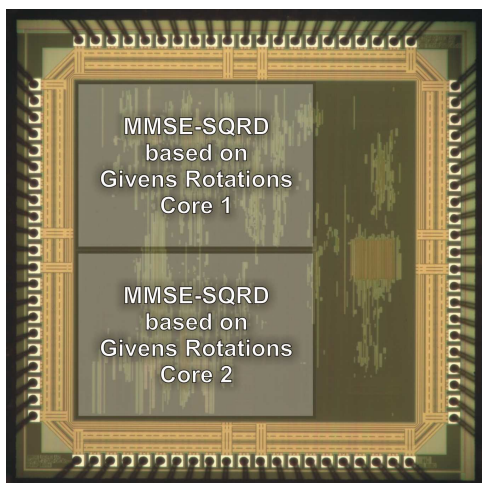
### Description

- IEEE 802.11n-compliant programmable low-density parity check (LDPC) decoder

### Technical Data

- Process: UMC 0.18  $\mu\text{m}$  1P/6M CMOS technology
- Clock: 208 MHz
- Area: 3.39 mm<sup>2</sup>
- Throughput: 780 Mbit/s

## MMSE Sorted QR Decomposition



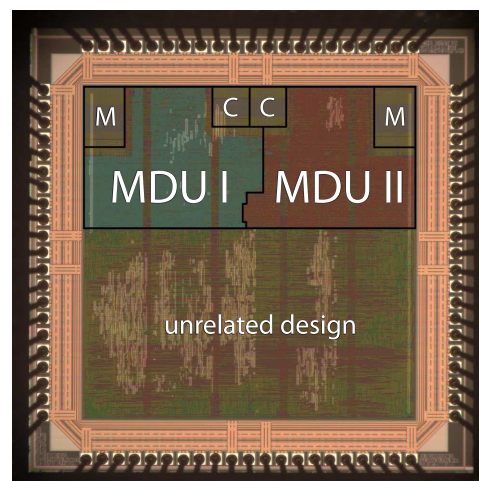
### Description

- MMSE sorted QR decomposition based on Givens rotations

### Technical Data

- Process: UMC 0.18  $\mu\text{m}$  1P/6M CMOS technology
- Clock: 152 MHz
- Total Area: 2.28 mm<sup>2</sup> (four different architectures)
- Delivers up to 3.8 M SQRD/s

## Singular Value Decomposition Processors



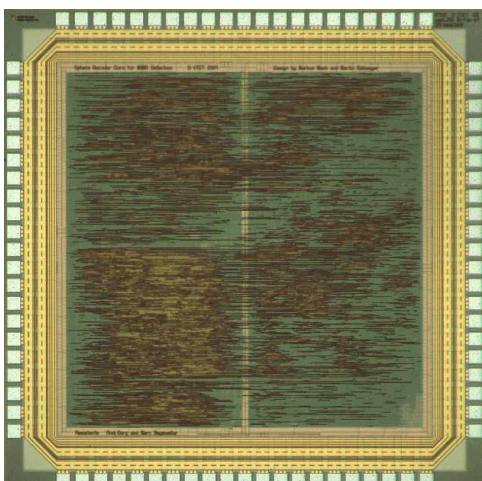
### Description

- First singular value decomposition ASIC for MIMO communication

### Technical Data

- Process: UMC 0.18  $\mu\text{m}$  1P/6M CMOS technology
- Clock: MDU-I 133 MHz / MDU-II 272 MHz
- Area: 0.41 mm<sup>2</sup> / 0.37 mm<sup>2</sup>
- 86.4 kSVD/s / 63.2 kSVD/s

## Hard-Output Sphere Decoder



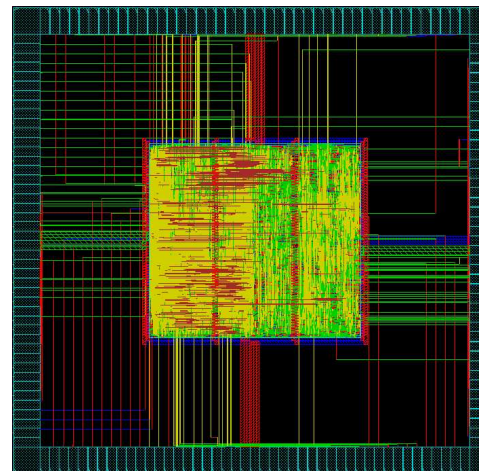
### Description

- First 4-stream hard-output sphere decoder ASIC

### Technical Data

- Process: UMC 0.25  $\mu\text{m}$  1P/5M CMOS technology
- Clock: 57 MHz
- Area: 117 k gate equivalents
- Achieves 75 Mbit/s at 20 dB SNR

## Soft-Output STS Sphere Decoder



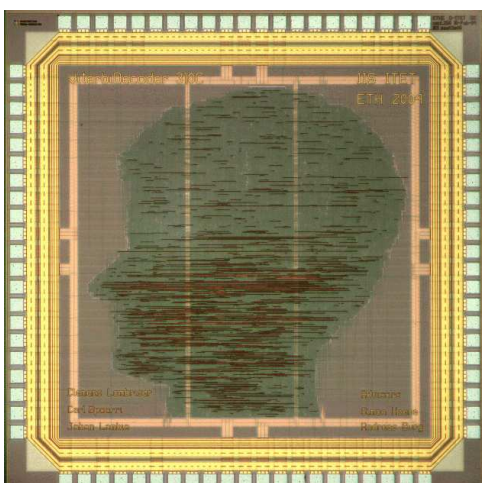
### Description

- First 4-stream soft-output sphere decoder based on the single tree search (STS) strategy

### Technical Data

- Process: UMC 0.25  $\mu\text{m}$  1P/5M CMOS technology
- Clock: 71 MHz
- Area: 1.9 mm<sup>2</sup>
- Throughput ranges from 10 Mbit/s to 95 Mbit/s

## Viterbi Decoder for MIMO WLAN



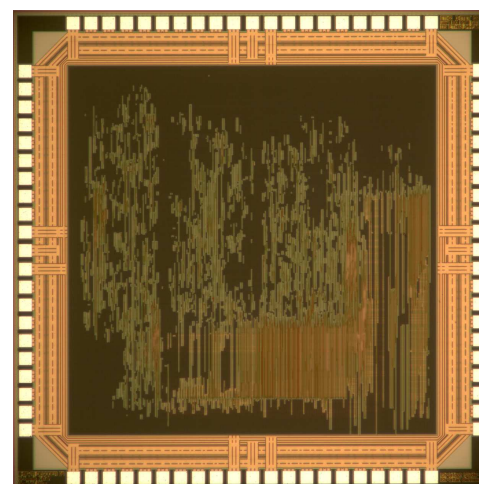
### Description

- IEEE 802.11n-compliant Viterbi decoder ASIC

### Technical Data

- Process: UMC 0.25  $\mu\text{m}$  1P/5M CMOS technology
- Clock: 310 MHz
- Area: 1.7 mm<sup>2</sup>
- Designed for 310 Mbit/s throughput

## BCJR Decoder for Iterative MIMO Detection



### Description

- First 64-state BCJR decoder for iterative MIMO detection

### Technical Data

- Process: UMC 0.18  $\mu\text{m}$  1P/6M CMOS technology
- Clock: 375 MHz
- Area: 2.95 mm<sup>2</sup>
- Throughput: 375 Mbit/s